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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,198	12/28/2001	Jong Dae Kim	0465-0883P	5402

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EXAMINER	
NELSON, ALECIA DIANE	

ART UNIT	PAPER NUMBER
2675	5

DATE MAILED: 03/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,198	KIM, JONG DAE	
	Examiner	Art Unit	
	Alecia D. Nelson	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/06/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 01/06/04. These drawings are approved by the examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. ***Claims 1, 3-5, 7-9, and 11-16*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchino (U.S. Patent No. 6,040,816) in view of Nakano et al. (U.S. Patent No. 6,529,181).

With reference to **claims 1, 11, and 16,** Uchino teaches an LCD device comprising a LCD panel (see Figure 1); a plurality of source drivers (20) applying data signals to the LCD panel; a plurality of gate drivers (10) applying gate driving signals to the LCD panel (see column 1, lines 29-56); an external source providing at least two clock signals (HCK, HCKX) having different phases and data (B1-B3) synchronized with each output signal (see Figure 1, column 1, line 57-column 2, line 43).

Uchino fails to specifically teach that the clock signals are input to the source drivers from a timing controller, however does teach that the clock signals are input to the source drivers as explained above. Uchino also fails to specifically teach the usage of two data buses transmitting data from the external device to the drivers. With reference to **claims 11 and 16,** Uchino also fails to teach that the data synchronized with the respective clock signal for each odd/even numbered data or R/G/B data through different data busses.

Nakano et al. teaches a liquid crystal display apparatus including an timing controller (100) which outputs timing control signal (D1), clock signal (D4, 131) and clock signal (D5, 132) to the drain drivers along with a data bus (134), as well as R/G/B display data (see column 6, lines 22-29). Nakano et al. also teaches the usage of one main data bus (134), which divides into individual buses into each of the drain drivers (130) (see Figure 1). With further reference to *claims 11 and 16,* Nakano et al. also teaches that the first clock signal (D4) is transmitted to odd-numbered drain drivers (130) and clock signal (D5) is transmitted to even numbered drain drivers (130) (see column 6, lines 38-43).

Therefore it would have been obvious to one having ordinary skill in the art that the control data is applied to the liquid crystal panel by usage of a controlling device which supplies timing control signals, clock signals, R/G/B data to odd/even drain groups as taught by Nakano et al., the controlling device being the external device as taught by Uchino, thereby providing a display wherein the clock and data signals are

inverted with relation to one another in order to reduce noise generated, which improves the overall resolution of the display device.

With reference to **claims 3, 4, 7, 8, 12, and 14,** Uchino teaches that the data is synchronized with a rising edge time and falling edge time of each clock signal (see Figure 2).

With reference to **claim 5,** Uchino teaches that the clock signals (HCK, HCKX) are opposite phase to each other (see column 2, lines 8-15).

With reference to **claim 9,** Uchino teaches that the data is synchronized with the rising and falling edges of the clock signals, as explained above, however fails to teach that the data is split into odd and even groups.

Nakano et al. teaches a first clock signal (D4) for driving odd drain drivers and a second clock signal (D5) for driving even drain drivers (see column 6, lines 38-43).

Therefore it would have been obvious to one having ordinary skill in the art to drive odd and even display data as taught by Nakano et al. in a system which allows for synchronization as taught by Uchino in order to reduce the amount of crosstalk and thereby enhancing the resolution of the liquid crystal panel.

With reference to **claim 13 and 15,** Uchino teaches that the source driver samples data (A1-A3) synchronized with a rising edge of the data synchronized with a falling edge of each clock signal that is output (see Figure 2).

4. ***Claims 2, 6, and 10*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchino and Nakano et al. as applied to claim 1 above, and further in view of Itakura(U.S. Patent No. 5,252,957).

With reference to **claim 2, 6, and 10** Uchino and Nakano et al. teach synchronizing the data with the clock signals, however fail to specifically teach that the number of data busses is in proportion to the number of clock signals.

Itakura teaches an AMLCD wherein three busses carry three clock signals (CK1-3) and three different busses carry video data R, G, and B (see Figure 1). With further reference to claim 6, it is taught that the three clock signals have different phases to one another (see Figure 3).

Therefore it would have been obvious to one having ordinary skill in the art to allow the usage of the same amount of data busses as clock busses as taught by Itakura in a device similar to that which is disclosed by Uchino and Nakano

Response to Arguments

5. Applicant's arguments filed 1/06/04 have been fully considered but they are not persuasive.

The applicant argues that Uchino fails to teach the timing controller which feeds both clock signals and image data to the source drivers, wherein the timing controller of Uchino would be represented by the logical circuits, which is provided at a different location that that of the timing controller in the claimed invention. However, the examiner admits that Uchino fails to teach the usage of the timing controller. Further, there is no reference made by the examiner that the logical circuits act as a timing controller, nor is there any disclosure with reference to Figure 1, explaining that the logical circuits act as a timing controller. Also, the claims do not recite that the timing controller (47) feeds clock signals aw well as image data to the source driver as argued by the applicant. Therefore, the arguments made about the positioning of the control circuit of Nakano, which operates as the timing controller, being different in location to the logical circuits of Uchino is irrelevant. Uchino teaches that the clock signals are provided from an external source and Nakano teaches that the signals are provided from an external source (computer) through an interface, which comprises a control circuit. Therefore, a person having ordinary skill in the art could combine Uchino and Nakano to produce the invention as recited in the claims. The applicant also argues unexpected results over Uchino. However, the applicant is arguing the applied rejection singularly, as opposed to the combined teachings of the two references used. Uchino does teach disadvantages resulting in reduction of resolution and occurrence of ghost

images, however solves the problem by providing a phase adjustment of the sampling pulses according to the secondary clock signals. Nakano teaches reducing the clock signal frequency in order to reduce electromagnetic interference. Therefore, there are no unexpected results over the combination of the references.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703) 305-0143. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras can be reached on (703) 305-9720. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

adn/ADN
March 10, 2004

Amr Ahmed Awad